**PROFESSIONAL EXPERIENCE**

**Moxa |** *Embedded Software Engineer* Taipei, Taiwan

**Languages:** *C, Shell Scripts, HTML, JavaScript* **Jun. 2021 – Oct. 2024**

**Technologies & Tools:** *Linux, TCP/IP, SQLite, Makefile, I2C, UART, GitLab(CI/CD pipelines), Docker, Jira*

* Protocol Gateways (based on Linux):  
  Achieved USD 3M/year revenue with +10% YoY growth (2021 - 2024)
  + Led modularization of the IEC 60870-5-101/104 protocol stack for [MGate 5192](https://www.moxa.com/en/products/industrial-edge-connectivity/protocol-gateways/modbus-tcp-gateways/mgate-5192-series) to improve maintainability and scalability, cutting integration time for new products by over 50%
  + Built a customized full-stack solution for serial configuration and troubleshooting on [MGate 5216](https://www.moxa.com/en/products/industrial-edge-connectivity/protocol-gateways/modbus-tcp-gateways/mgate-5216-series), enabling customer onboarding and reducing debugging time between software R&D and clients by over 90%
  + Improved the RESTful library for the MGate 5000 series using an IPC-based design, reducing API maintenance and development time by 10%
  + Developed unit tests and valgrind scripts for MGate 5000 series software modules integrated with GitLab CI, enhancing system stability and enabling early detection of memory issues with 90% test coverage
  + Co-developed the SD card backup module with the Linux kernel team and independently resolved issues through kernel source code analysis
* Media Converters (based on MCUs):
  + Led the software development of [IMC-P21A-G2](https://www.moxa.com/en/products/industrial-network-infrastructure/ethernet-media-converters/ethernet-to-fiber-media-converters/imc-p21a-g2-series) (Ethernet-to-fiber) from project initiation to market launch
  + Resolved sample point and communication issues for Japanese clients using [ICF-1171I](https://www.moxa.com/en/products/industrial-edge-connectivity/serial-converters/fieldbus-to-fiber-converters/icf-1171i-series) (CAN-to-fiber)

**EDUCATION**

**University of Washington**  Seattle, WA

Master of Science in Electrical and Computer Engineering **Sep. 2025 – June 2027**

**National Taiwan University of Science and Technology |** GPA: 3.92/4.3 Taipei, Taiwan

Master of Science in Electrical Engineering (Mobile Communication Specialization) **Sep. 2018 – Aug. 2020**

**Chang Gung University |**  GPA: 3.7/4.0Taoyuan, Taiwan

Bachelor of Science in Electrical Engineering (IC Design Specialization) **Sep. 2014 – Jun. 2018**

**PROJECTS**

**Analysis of Call Admission Control Schemes for Secondary Users in CRN** – *M.S. Thesis* **Sep. 2019 – Aug. 2020**

* Proposed a novel access mechanism for cognitive radio networks (CRN), combining spectrum leasing, channel aggregation and hand-offs to improve spectrum utilization, achieving lower user delay and higher throughput

**Intelligent Curtain System** – *Undergraduate* *Capstone Project* **Jul. 2016 – Jun. 2017**

Award: first place in the final project exhibition

* Created an intelligent curtain system using [SmartServer](https://www.enocean.com/en/product/smartserver-iot/) and Zigbee sensors with Power Line Communication, enabling automatic adjustment based on illumination levels
* Designed and implemented a curtain control PCB using D flip-flops, BJTs and RLC components, completing the entire process from circuit design to soldering to ensure seamless system integration
* Programmed Zigbee firmware to ensure accurate storage of temperature and brightness data in the SmartServer

**Knowledge Discovery in Database (KDD) Cup Contest** **Feb. 2019 – Jun. 2019**

Result: weighted F1-score of 0.6884 on the test set, close to the first-place team’s score of approximately 0.7

* Developed machine learning workflows in Python, including preprocessing, feature engineering, and model training, to predict Baidu Map users’ preferred transportation modes using 500,000+ data points

**RTOS Implementation Sep. 2018 – Jan. 2019**

* Modified the μC/OS-II kernel scheduling to implement and evaluate various scheduling algorithms, including Earliest Deadline First Scheduling, Non-Preemptible Critical Sections and Priority Ceiling Protocol

**FPGA System Design Lab Sep. 2017 – Jan. 2018**

* Implemented a 2D LED dodging game using Verilog on an FPGA Development Board